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ABSTRACT OF THE DISCLOSURE

A ~~The~~ semiconductor integrated circuit is provided with a plurality of sub reset signal generators and a main reset signal generator. The sub reset signal generators respectively generate sub power-on reset signals whose timings differ from each other. The main reset signal generator generates a main power-on reset signal according to at least one from any of the sub power-on reset signals. Therefore, even where the characteristics of elements constituting the semiconductor integrated circuit change due to changes in the manufacturing conditions of the semiconductor integrated circuit, one of the sub power-on reset signals is generated at a normal timing. As a result, the main reset signal generator is able to generate a main power-on reset signal by using a normal sub power-on reset signal. That is, it is possible to constitute a power-on resetting circuit having a wide operation margin, wherein the internal circuits can be initialized without fault.